REMARKS

In the last Office Action, the Examiner objected to the abstract of the disclosure as containing an informality. Claims 1-3 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Publication No. 2002/0000858 A1 to Lu. Additional art was cited of interest.

In accordance with the present response, the specification has been suitably revised to correct informalities, provide antecedent basis for the claim language, and bring it into better conformance with U.S. practice. Original claims 1-3 have been replaced by new claims 4-16 to further patentably distinguish the claims from the prior art of record, provide a fuller scope of coverage, and otherwise bring the claims into better conformance with U.S. practice. The title of the invention has been changed to "FLIP-FLOP CIRCUIT, SHIFT REGISTER HAVING FLIP-FLOP CIRCUITS, AND METHOD OF OPERATING FLIP-FLOP CIRCUIT AND SHIFT REGISTER" to more clearly reflect the invention to which the new claims are directed. A new, more descriptive abstract which overcomes the objection raised by the Examiner has been substituted for the original abstract.

In view of the foregoing, applicant respectfully submits that the objection to the abstract has been overcome and should be withdrawn.

Applicant respectfully submits that the prior art of record does not disclose or suggest the subject matter recited in newly added claims 4-16.

As described in the specification (pgs. 1-2), conventional flip-flop circuits contain a large number of elements required to generate a steady-state output signal having either a high or low potential. Thus, operation of the conventional flip-flop circuits has resulted in an increase in power consumption and a decrease in the performance of the flip-flop circuits.

The present invention overcomes the drawbacks of the conventional art by providing a flip-flop circuit and a method for operating the flip-flop circuit which improves flip-flop performance and reduces power consumption.

New independent claim 4 is directed to a flip-flop circuit. With reference to the embodiment shown in Figs. 1-3, the flip-flop circuit has a data input terminal D and a first switching element 1 having a first terminal connected to the data input terminal D, a second terminal, and a first gate for receiving a first control signal CX. A first inverter element 2 has an input terminal connected to the second terminal of the first switching element 1. A second switching element 3 has a first terminal connected to an output terminal of the first inverter element 2, a second terminal, and a second gate

for receiving a second control signal C. A second inverter element 4 has an input terminal connected to the second terminal of the second switching element 3 and a data output terminal Q.

According to the present invention, the flip-flop circuit has signal generating means (e.g., circuit shown in Fig. 2) for generating the first and second control signals CX and C and for inputting the first and second control signals CX and C to the first and second gates of the first and second switching elements 1, 3, respectively, to simultaneously activate the first and second switching elements 1, 3 for initializing the flip-flop circuit and to alternately activate the first and second switching elements 1, 3 for activating the flip-flop circuit. By this construction, initialization and activation of the flip-flop circuit is accomplished with a reduced number of parts (e.g., a reduced number of transistors) as compared to the conventional art.

In another aspect embodied in new independent claim 9, the present invention is directed to a method for operating a flip-flop circuit. According to the method of the present invention, as shown in Fig. 3, the flip-flop circuit is initialized by inputting first and second control signals to the first and second gates of the first and second switching elements, respectively, to simultaneously activate the first

and second switching elements. The flip-flop circuit is then activated by inputting the first and second control signals to the first and second gates of the first and second switching elements, respectively, to alternately activate the first and second switching elements.

In yet another aspect, as embodied in new independent claim 13, the present invention is directed to a method for operating a shift register having a plurality of flip-flop circuits connected together. According to this method, the shift register is initialized by inputting first and second control signals to the first and second gates of the first and second switching elements, respectively, of each of the flip-flop circuits to simultaneously activate the first and second switching elements. The shift register is then activated by inputting the first and second control signals to the first and second gates of the first and second switching elements, respectively, of each of the flip-flop circuits to alternately activate the first and second switching elements.

By the foregoing methods recited in new independent claims 9 and 13, the performance of the flip-flop circuit is improved and power consumption is substantially reduced as compared to the conventional art.

The prior art of record does not disclose or suggest the structural combination of the flip-flop circuit recite in

independent claim 4, the method for operating the flip-flop circuit recited in independent claim 9, and the method of operating the shift register recited in independent claim 13. For example, the reference to Lu cited by the Examiner discloses a flip-flop circuit 300 having switching elements 312, 318, a data input terminal Din, a data output terminal Qout, inverters 302, and MOS transistors 306, 308 for receiving control signals CLKiB and CLKi (Fig. 2).

However, Lu does not disclose or suggest the specific structural combination of the flip-flop circuit recited in claim 4, namely, signal generating means for generating the first and second control signals and for inputting the first and second control signals to the first and second gates of the first and second switching elements, respectively, to simultaneously activate the first and second switching elements for initializing the flip-flop circuit and to alternately activate the first and second switching elements for activating the flip-flop circuit. For example, Lu does not disclose or suggest an operation to initialize the flip-flop circuit 300 by the input of control signals to simultaneously activate the switching elements 312, 318.

However, Lu does not disclose or suggest the specific steps for operating the flip-flop circuit recited in claim 9, namely, the steps of initializing the flip-flop

circuit by inputting first and second control signals to the first and second gates of the first and second switching elements, respectively, to simultaneously activate the first and second switching elements, and activating the flip-flop circuit by inputting the first and second control signals to the first and second gates of the first and second switching elements, respectively, to alternately activate the first and second switching elements. Lu does not disclose or suggest an operation to initialize the flip-flop circuit 300 by the input of control signals to simultaneously activate the switching elements 312, 318. Independent claim 13 similarly patentably distinguishes from Lu.

Claims 5-8, 10-12 and 14-16 depend on and contain all of the limitations of independent claims 4, 9 and 13, respectively, and, therefore, distinguish from the prior art of record at least in the same manner as claims 4, 9 and 13.

In view of the foregoing amendments and discussion, the application is believed to be in allowable form. Accordingly, favorable reconsideration and allowance of the claims are most respectfully requested.

Respectfully submitted,

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